EXAMINER'S AMENDMENT

1. An extension of time under 37 CFR 1.136(a) is required in order to make an examiner's amendment which places this application in condition for allowance. During a telephone conversation conducted on April 25, 2008, the Examiner requested an extension of time for one MONTH(S) and authorized the Director to charge Deposit Account No. 50-1147 the required fee of $ 120:00 for this extension and authorized the following examiner's amendment. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2.

The application has been amended as follows: amend claim 15 as below:

Claim 15: (Currently amended) A circuit board connection structure for connecting a first circuit board in which a thermoplastic resin is used as an insulating material to a second circuit board serving as a mother board, wherein

said first circuit board has a multilayer structure wherein insulating layers made only from a thermoplastic resin and interconnection layers are stacked alternately and to electrically connect adjacent interconnection layers together an interlayer connection material is disposed in said insulating layers,

in an insulating layer being made only from the thermoplastic resin and constituting a connection face of said first circuit board to be connected to said second

circuit board, via holes reaching the inner interconnection layers are formed, said via holes being filled with a connection material,

said second circuit board has a multilayer structure wherein insulating layers and interconnection layers are stacked alternately and an interlayer connection material for electrically connecting adjacent interconnection layers together is disposed in said insulating layers,

at least lands serving as connection terminals are formed on a connection face of said second circuit board, and inner interconnection layers are used for interconnecting said lands,

said first circuit board is connected to said second circuit board by said connection material of the first circuit board being electrically connected to the lands of said second circuit board and the insulating layer constituting the connection face of said first circuit board being adhered to the connection face of said second circuit board by thermal welding, and

wherein ~~when~~ the insulating layers of said second circuit board are made from a thermoplastic resin, ~~as~~ and the thermoplastic resin constituting the insulating layers of the first board~~,~~ comprises a thermoplastic resin material having a lower melting point than the thermoplastic resin constituting the insulating layers of said second circuit board ~~is used~~.

3. The following is an examiner's statement of reasons for allowance:

4. Regarding claims 1-8, 11 and 29-32:

A circuit board having a flat plate shaped first board part and a second flat plate shaped second board part disposed stacked on a partial region of the this first board part with limitations "a plurality of second interconnection patterns are disposed on said stacked region of said second board part so as to form pairs with said plurality of first interconnection patterns, and between the pairs of said first interconnection patterns and said second interconnection patterns, interboard connection parts are formed from a connection material which at a temperature applied to melt the thermoplastic resin melts at least partially and electrically connects the first and second interconnection patterns together," in combination with other claimed limitations of the base claim 1 are not disclosed or fairly suggested by prior art of record taken alone or in combination.

5. Regarding claims 12 and 13:

A circuit board having a flat plate shaped first board part and a second flat plate shaped second board part disposed stacked on a partial region of the this first board part with limitations "a plurality of second interconnection patterns are disposed on said stacked region of said second board part so as to form pairs with said plurality of first interconnection patterns, between the pairs of said first interconnection patterns and said second interconnection patterns, interboard connection parts are formed from a connection material which at a temperature applied to melt the thermoplastic resin melts

at least partially and electrically connects the first and second interconnection patterns together," in combination with other claimed limitations of the base claim 12 are not disclosed or fairly suggested by prior art of record taken alone or in combination.

6. Regarding claim 15:

A circuit board connection structure for connecting, a first circuit board in which a thermoplastic resin is used as an insulating material to a second circuit board serving as a mother board with the limitation "wherein the insulating layers of said second circuit board are made from a thermoplastic resin, and the thermoplastic resin constituting the insulating layers of the first board comprises a thermoplastic resin material having a lower melting point than the thermoplastic resin constituting the insulating layers of said second circuit board" in combination of other claimed limitation of the claim has not been disclosed or fairly suggested by the prior art of record.

7. Regarding claim 16:

A circuit board connection structure for connecting, a first circuit board in which a thermoplastic resin is used as an insulating material to a second circuit board serving as a mother board with the limitation "said connection material includes at least a tin component and a metal component with a higher melting point than the tin component, and is electrically connected to the lands of said second circuit board by the tin component diffusing into the lands" in combination with other claimed limitations of the

claim has not been disclosed or fairly suggested by prior art of record taken alone or in combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ibp
April 25, 2008

/Ishwar (I. B.) Patel/
Primary Examiner, Art Unit 2841